Power Integrity Templates for the QUCS simulator program.

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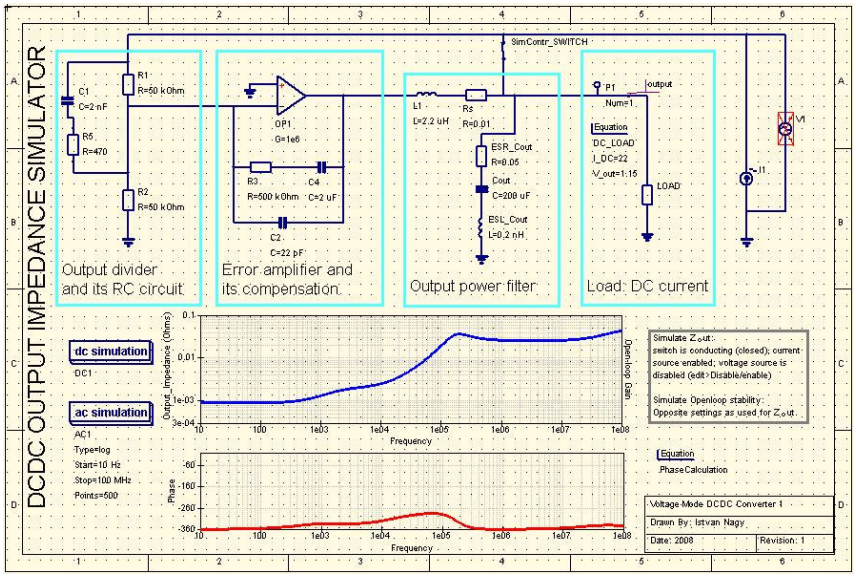
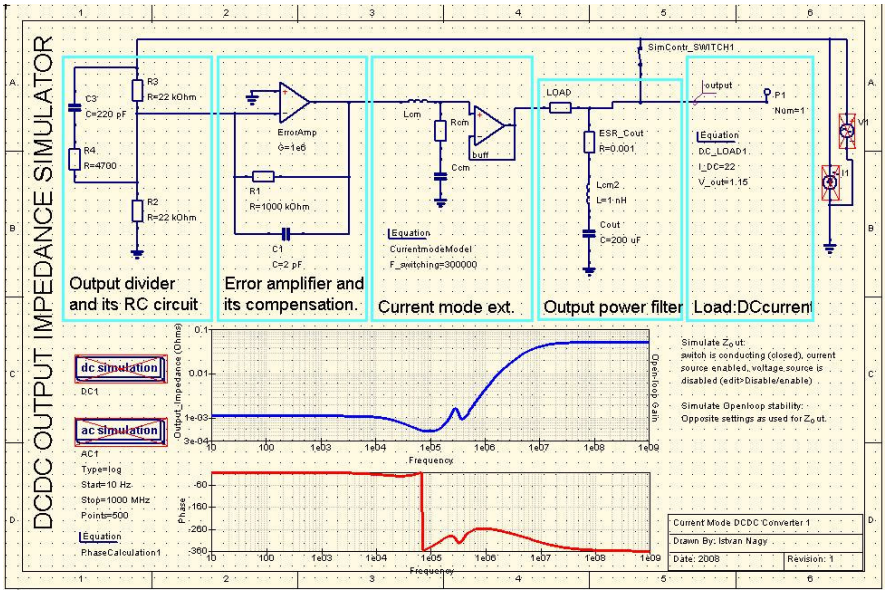
With these templates, you can set up a model easily and quickly for your power distribution system based on macromodelling and using the Quite Universal Circuit Simulator program. (http://qucs.sourceforge.net/)

To start, open the QUCS program, and select Project>OpenProject. Then select the containing folder (PowerIntegrityDesign_prj) in the browser. Then in the left panel>Content>Schematics>filename to open a schematics drawing. There are 3 schematics drawings. One is the main simulation top level schematic (Powerintegrity.sch), which can include one of the other 2 schematics drawings as sub circuits in its model. The other 2 are for separately model the used DCDC converter in the system. There can be 2 types (so 2 schematic pages are provided), a Current mode controlled and a voltage mode controlled.

1. **DCDC converter model**: Select the one which reflects the control method of your used DCDC controller: Current or voltage mode, so 2 templates are provided. Then open the schematic from the left panel >content>schematics>filename (double-click). Edit the circuit parameters. Important at this point is that this page does not contain the actual schematics of your DCDC converter, but creates a model which reflects its behaviour in the frequency domain (for example, the switching circuits are not included). It has R/L/C elements. You have to provide their value to the QUCS template, based on the real schematics of the DCDC. You can locally simulate the DCDC converter for open-loop bode diagram (simulation selector switch is not conducting, current source is disabled) or for closed loop Impedance characteristics (switch is conducting and voltage source is disabled). To simulate here, you have to enable the simulations (by selecting Edit>Deactivate/Activate and click on the DC simulation icon and AC simulation icon, and clicking twice on the I1 current source or the U1 voltage source), then click on the cogwheel icon to simulate. You can open the control loop for a Bode type simulation of the control loop by the switch on the top. When you want to simulate the top-level system, the DCDC controller page must be like this: switch is closed, simulations disabled, then file saved. The DCDC schematic page has to be referenced in the main page (powerintegrity.sch). This can be done this way: on the main page, delete the already included model (click on it, then DEL key), then click once on the filename of the DCDC page on the left panel >content>schematics>filename then a small box is attached to the cursor. Put it down into its place in the top schematics.



Voltage mode DC/DC model

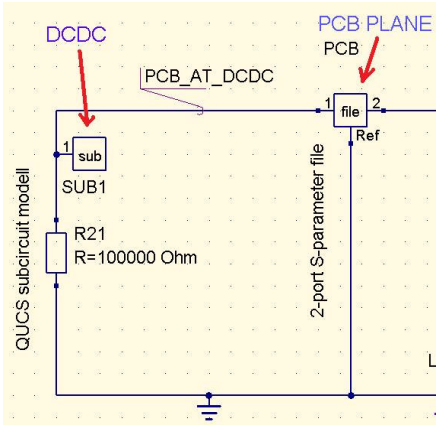


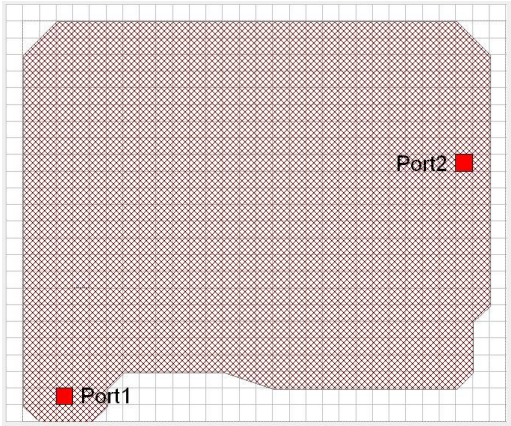
Current mode DC/DC model

The current mode DCDC converter model is not as straightforward as the model for the voltage mode converter, since it has a very tricky mode of operation. By definition, a current mode converter has a double pole at the F=F_switching/2 and a single pole at the F=1/(2*TT*R_load*Cout). To model this, I have created the above AC small signal substitution circuit model, for simulation. It is not proven that it is correct, but it reflects the 2 poles given by definition and it should behave the same way in the AC simulation, as the original DC/DC converter does. Obviously it would not be possible to simulate all the switching circuits in the AC analysis, so instead of that, a model was created. Some circuit parameters are set automatically when the user sets the required input parameters about the load and switching frequency.

The user can chose which topology of converter to substitute into the system level simulation.

2. **PCB Power plane simulation model:** We have to simulate the PCB power plane with another program, like the free Sphinx-student program (www.powerintegrity.net) to generate an S or Z-parameter (Touchstone) file. The result file can be used as a macro model of the power/gnd plane pair in SPICE-like simulation programs, like the QUCS program. In the actual (0.14) version of the QUCS, we can do only AC simulation (frequency domain impedance) when using touchstone-based models. To be able to do transient simulation (time domain noise), we need to use RLGC-based spice circuit models instead. When you generated the touchstone file (.s2p extension), then you have to add it to the circuit element, representing the power/gnd plane pair. The simulation is advised to be done with 2 ports, one at the DCDC converter, one at the IC package. You can use more ports, for example to take the decoupling capacitor placement into account, but then you have to manage to connect them in the QUCS schematic.





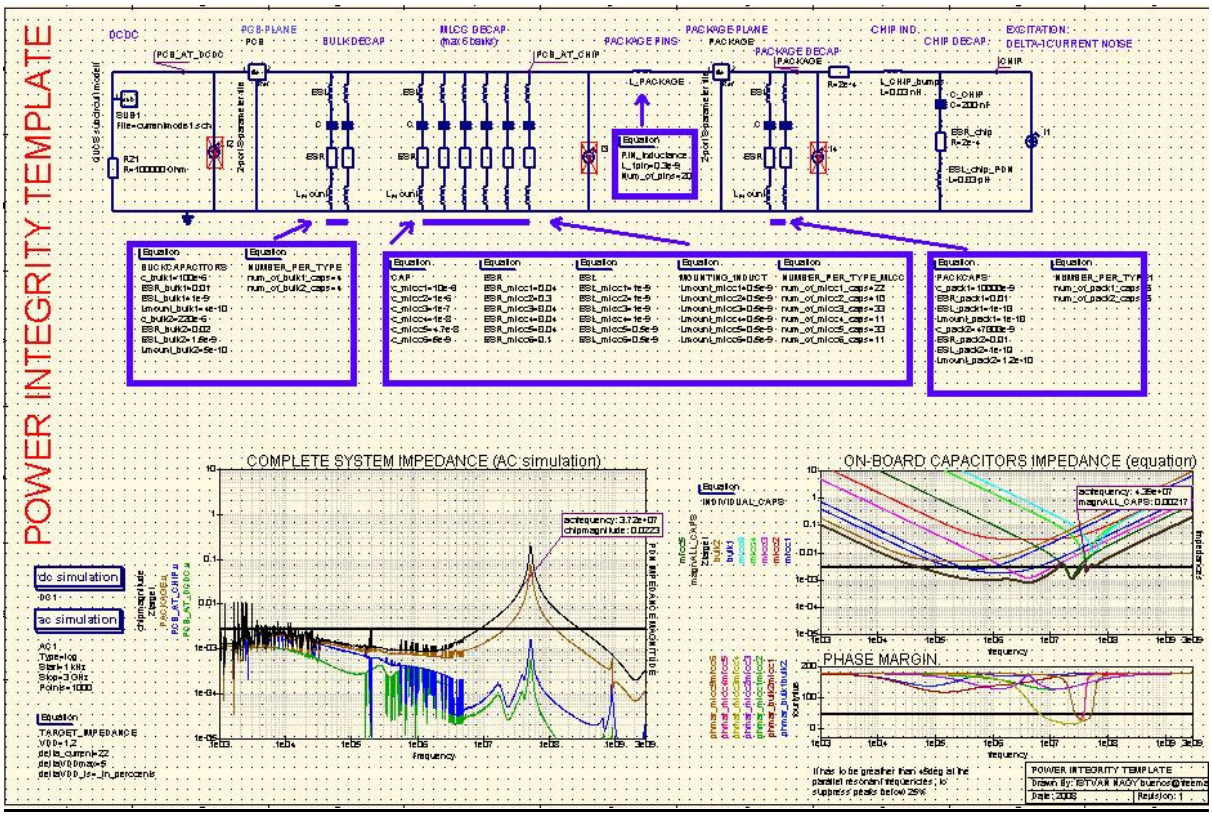
3. **IC Package model:** Since the IC manufacturers don't provide anything about it, we have to guess, and create the model in the same way as the PCB model. Normally suitable assumptions: Create a rectangular plane pair at a size of the package, with plane separation of 50um. Put 2 ports: one in the middle, one close to a corner. This model is very inaccurate, but much better than nothing.

4. **Other Package and chip parameters:** Pin inductance and on-package decoupling capacitor parameters. These are not given from the manufacturers, since normally they treat it as a top secret. So we have to guess again.

5. **On board decoupling capacitors:** The used capacitors parameters are needed here. Specify them in the given text fields, not directly on the components. The mounting inductances of the capacitors can be estimated by equations, or practical numbers, but the best is to simulate them using a 3D full electromagnetic field-solver program, like the free/opensource Fasthenry. Fasthenry is a command line program so not very user friendly. The package from www.fastfieldsolvers.com contains a text editor and a 3D model display helping creating the Fasthenry models for EM simulation.

6. **Simulations:** The full system simulation has to be done on the Powerintegrity.sch schematics page, by opening it and clicking on the cogwheel icon  . In the given files, the result will appear on the same page as the schematics drawings, so you have to go back to ait after simulation has done. Before this, you should set up the target impedance requirement by providing parameters into the equation box in the bottom left corner: VDD, delta VDD (maximum allowed in %) and delta current noise (estimated maximum in Amps). There are several excitation sources in the schematics, but only one can be enabled at one time. To enable or disable one: use the edit>disable/enable menu then click on the object (this case onto the current source). Normally the most important is to maintain a good impedance profile seen from the chip, so to check it enable the source connected to the chip node and disable all the others. You can see the impedance profiles of other nodes too, but seen from the selected node. To see the accurate impedance profile of another node (example on the PCB at the package), you have to enable the current excitation source connected to that node (and disable all the others), then run the simulation. The on-board decoupling network impedance profile is provided separately from the main AC simulation, just by embedded equations.

Design: You have to adjust the decoupling capacitor parameters, the number of capacitors/bank (1 bank is all same type capacitors), the PCB power planes, the DCDC converter output filter and compensation schemes, and package decoupling capacitors to push your system impedance profile seen from the chip below the target impedance line on the graphs.



Advanced design: You can simulate your power/ground plane pairs and the package with multiple ports. For example you can provide ports at the decoupling capacitor locations, or at each package pin to make the simulation to be more accurate and to take the decap locations into account. Then you have to add the simulated/generated s-parameter file into the drawing, from the left panel>components>file components>n-port s-parameter file. And rearrange the schematic page with the proper connections.